MOTOROLA

Professional Radio
GM Series

LB1 (29.6 - 36.0MHz)

LB2 (36.0 - 42.0MHz)

LB3 (42.0 - 50.0MHz)

Service Information

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Computer Software Copyrights

Table of Contents

Chapter 1 MODEL CHART AND TECHNICAL SPECIFICATIONS

Chapter 2 THEORY OF OPERATION

Chapter 3 TROUBLESHOOTING CHARTS

Chapter 4 Low Band PCB/SCHEMATICS/PARTS LISTS

Chapter 1

MODEL CHART AND TECHNICAL SPECIFICATIONS

1.0 GM360 Model Chart

GM Series Low Band 29-50 MHz				
Model				Description
MDM25BKF9AN5_E				GM360 LB1, 29.0-36.0 MHz, 25-60W, 255 Ch
	MDM25CKF9AN5_E			GM360 LB2, 36.0-42.0 MHz, 25-60W, 255 Ch
		MDM25DKF9AN5_E		GM360 LB3, 42.0-50.0 MHz, 25-60W, 255 Ch
			Item	Description
X	X	X	GCN6114_	Control Head, GM360
X			IMUB6003_S	Field Replaceable Unit (Main Board) GM360
	X		IMUB6004_S	Field Replaceable Unit (Main Board) GM360
		X	IMUB6005_S	Field Replaceable Unit (Main Board) GM360
X	X	X	ENBN4056_	Packaging, Waris Mobile
X	X	X	HKN9402_	12V Power Cable
X	X	X	MDRMN4025_	Enhanced Compact Microphone
X	X	X	RLN4774_	3 Point Mount
X	X	X	6864110B81_	User Guide, GM360

X = Indicates one of each is required

2.0 Technical Specifications

Data is specified for +25°C unless otherwise stated.

General Specifications	
Channel Capacity **GM360**	 255
Power Supply	13.2Vdc (10.8 - 15.6Vdc)
Dimensions: H x W x D (mm) Height excluding knobs	**GM360** 59mm x 179mm x 250mm (add 9mm for Volume Knob)
Weight	2064gr
Sealing:	Withstands rain testing per MIL STD 810 C/D /E and IP54
Shock and Vibration:	Protection provided via impact resistant housing exceeding MIL STD 810-C/D /E and TIA/EIA 603
Dust and Humidity:	Protection provided via environment resistant housing exceeding MIL STD 810 C/D /E and TIA/EIA 603

Transmitter	LB1	LB2	LB3
*Frequencies - Full Bandsplit	LB1 29.7-36.0 MHz	LB2 36.0-42.0 MHz	LB2 42.0-50.0 MHz
Channel Spacing	12.5/20/25 kHz	12.5/20/25 kHz	12.5/20/25 kHz
Frequency Stability (-30°C to +60°C, +25° Ref.)	±5.0 ppm	±5.0 ppm	±5.0 ppm
Power	25-60W	25-60W	25-60W
Modulation Limiting	±2.5 @ 12.5 kHz ±4.0 @ 20 kHz ±5.0 @ 25 kHz	±2.5 @ 12.5 kHz ±4.0 @ 20 kHz ±5.0 @ 25 kHz	±2.5 @ 12.5 kHz ±4.0 @ 20 kHz ±5.0 @ 25 kHz
FM Hum & Noise	-40 dB @ 12.5kHz -45 dB @ 20/25kHz	-40 dB @ 12.5kHz -45 dB @ 20/25kHz	-40 dB @ 12.5kHz -45 dB @ 20/25kHz
Conducted/Radiated Emission (ETS)	-26 dBm	-26 dBm	-26 dBm
Adjacent Channel Power	-60 dB @ 12.5 kHz -70 dB @ 25 kHz	-60 dB @ 12.5 kHz -70 dB @ 25 kHz	-60 dB @ 12.5 kHz -70 dB @ 25 kHz
Audio Response (300 - 3000 Hz)	+1 to -3 dB	+1 to -3 dB	+1 to -3 dB
Audio Distortion @1000Hz, 60% Rated Maximum Deviation	<3% typical	<3% typical	<3% typical

Receiver	LB1	LB2	LB3
*Frequencies - Full Bandsplit	LB1 29.7-36.0 MHz	LB2 36.0-42.0 MHz	LB2 42.0-50.0 MHz
Channel Spacing	12.5/20/25 kHz	12.5/20/25 kHz	12.5/20/25 kHz
Sensitivity (12 dB SINAD)	0.30 µV (0.22 µV typical)	0.30 µV (0.22 µV typical)	0.30 µV (0.22 µV typical)
Intermodulation (ETS)	>65 dB	>65 dB	>65 dB
Adjacent Channel Selectivity (ETS)	65 dB @ 12.5 kHz 75 dB @ 20 kHz 80 dB @ 25 kHz	65 dB @ 12.5 kHz 75 dB @ 20 kHz 80 dB @ 25 kHz	65 dB @ 12.5 kHz 75 dB @ 20 kHz 80 dB @ 25 kHz
Spurious Rejection (ETS)	75 dB @ 12.5 kHz 80 dB @ 20/25 kHz	75 dB @ 12.5 kHz 80 dB @ 20/25 kHz	75 dB @ 12.5 kHz 80 dB @ 20/25 kHz
Rated Audio	3W Internal 13W External	3W Internal 13W External	3W Internal 13W External
Audio Distortion @ Rated Audio	<3% typical	<3% typical	<3% typical
Hum & Noise	-40 dB @ 12.5 kHz -45 dB @ 20/25 kHz	-40 dB @ 12.5 kHz -45 dB @ 20/25 kHz	-40 dB @ 12.5 kHz -45 dB @ 20/25 kHz
Audio Response (300 - 3000Hz @ 20/25kHz) (300 - 2550Hz @12.5kHz)	+1 to -3 dB	+1 to -3 dB	+1 to -3 dB
Conducted Spurious Emission (ETS)	-57 dBm <1 GHz -47 dBm >1 GHz	-57 dBm <1 GHz -47 dBm >1 GHz	-57 dBm <1 GHz -47 dBm >1 GHz

*Availability subject to the laws and regulations of individual countries.

Chapter 2

THEORY OF OPERATION

1.0 Introduction

This Chapter provides a detailed theory of operation for the LowBand circuits in the radio. For details of the theory of operation and trouble shooting for the the associated Controller circuits refer to the Controller Section of this manual.

2.0 Low Band Receiver

2.1 Receiver Front-End

The low band receiver is bandsplit into three ranges depending on radio model, covering frequencies from 29.7 to 36.0 MHz, 36.0 to 42.0 MHz, or 42.0 to 50.0 MHz. The circuitry of the three models is identical except for component value differences. The receiver consists of five major blocks: front-end bandpass filters and pre-amplifier, first mixer, high-IF and blanker switches, low-IF and receiver back-end, and “Extender” (noise blanker). Two fixed-tuned bandpass filters perform antenna signal pre-selection. A cross over quad diode mixer converts the signal to the high - IF of 10.7 MHz. High-side first injection is used.

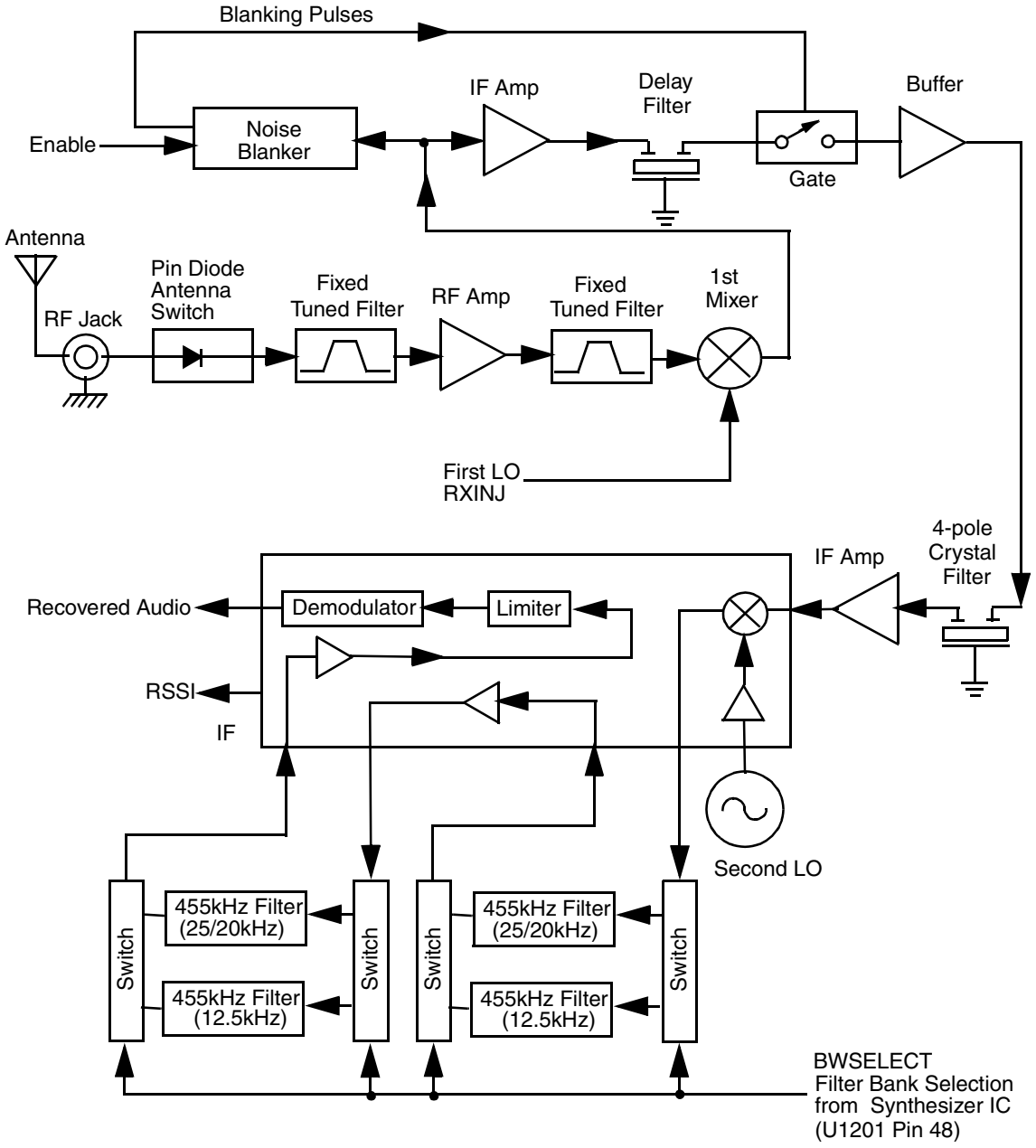


Figure 2-1 Low Band Receiver Block Diagram

There are two 2-pole 10.7 MHz crystal filters in the high-IF section and two switched pairs of 455 kHz ceramic filters in the low-IF section to provide the required adjacent channel selectivity. The second IF at 455 kHz is mixed, amplified and demodulated in the IF IC. The processing of the demodulated audio signal is performed by an audio processing IC located in the controller section.

2.2 Front-End Band-Pass Filters & Pre-Amplifier

The received signal from the radio's antenna connector is first routed through the harmonic filter and antenna switch, which are part of the RF power amplifier circuitry, before being applied to the receiver 5-pole antenna filter (L1001-L1005 and associated components). This filter configuration provides more rapid attenuation above the passband to provide better rejection of the half-IF spurious response. A dual hot carrier diode (D1001) limits any inband signal to 0 dBm to prevent damage to the RF pre-amplifier

The RF pre-amplifier is an SMD device (Q1001) with collector-base feedback to stabilize gain, impedance, and intermodulation. Transistor Q1002 compares the voltage drop across resistor R1005 with a fixed base voltage from divider R1006 and R1007, and adjusts the base current of Q1001 as necessary to maintain its collector current constant at 25 mA. Operating voltage is from the regulated 9.3V supply (9V3). During transmit, 9.1 volts (9T1) turns on both transistors in U1001, turning off Q1003 and therefore Q1001-2. This protects the RF pre-amplifier from excessive dissipation during transmit mode.

A second 5-pole fixed-tuned bandpass filter provides additional filtering of the amplified signal. This filter configuration also provides steeper attenuation above its passband for best half-IF attenuation.

2.3 First Mixer

The signal coming from the front-end is converted to the high-IF frequency of 10.7 MHz using a cross over quad diode mixer (U1051). The high-side injection signal (RXINJ) from the frequency synthesizer circuitry is filtered by a 7-pole low-pass filter (L1012-14 and associated circuitry) which removes second harmonic content from the injection signal and improves half-IF rejection. The 50-ohm output of the first mixer is applied to the input of the high-IF circuit block.

2.4 High Intermediate Frequency (IF) and Blanker Switches

The first mixer IF output signal (IF) is applied to a diplexer network consisting of L1101, L1111 and associated components. This network has three functions: it terminates the mixer output at frequencies other than 10.7 MHz into 51-ohm resistor R1101; it matches the 50-ohm mixer output to the first IF amplifier (Q1101) input; and it provides bandpass filtering at 10.7 MHz to prevent the 5.35 MHz half-IF component of the mixer output from creating a second harmonic at 10.7 MHz in Q1101, which degrades half-IF rejection.

The IF amplifier Q1101 uses ac and dc feedback to stabilize gain and quiescent current (approximately 28 mA). Operating voltage is from the regulated 9.3V supply (9V3). Its output is applied to a 10.7 MHz ceramic filter FL1101 which has a 3 dB bandwidth of 270 kHz and provides a time delay of 2.6 usec. This delay allows enough time for the "Extender" to respond to impulse noise present at the input of Q1101 and operate the blanker switches Q1102 and Q1103, muting the IF signal for the duration of the noise pulse. L1104 and L1105 also provide additional selectivity and time delay. Operation of the "Extender" circuit is explained in Section 8.5 below.

When the blanker switches turn "on" to mute the IF signal, they momentarily change the impedance of resonant circuits L1104 and L1105 from high to very low. This abrupt impedance change, if

presented to the high-Q crystal filters FL1102 and FL1103, would cause ringing of the filter response, stretching an otherwise narrow impulse into a long and audible output waveform. Therefore, source follower stage Q1104 isolates the blanker switches from the crystal filters, providing a consistent source impedance via matching network L1106, L1107 and associated components. Q1104 has unity voltage gain in this configuration.

Crystal filters FL1102 and FL1103 are 2-pole, 10.7 MHz units configured to provide an overall 4-pole response having a 3 dB bandwidth of approximately 12 kHz. The output is amplified by second IF amplifier Q1106 and applied to the low-IF circuitry, pin 1 of IF IC (U1103). A dual hot carrier diode (D1101) limits the amplifier output voltage swing to prevent overdriving the IF IC at RF input levels above -27 dBm.

2.5 Low Intermediate Frequency (IF) and Receiver Back End

The 10.7 MHz high-IF signal from the second IF amplifier feeds the IF IC (U1103) at pin1. Within the IF IC, the 10.7 MHz high -IF signal mixes with the 10.245 MHz second local oscillator (2nd LO) to produce the low-IF signal at 455 kHz. The 2nd LO frequency is determined by crystal Y1101. The low -IF signal is amplified and filtered by external pairs of 455 kHz ceramic filters (FL1105 and FL1107 for 20 kHz channel spacing, or FL1104 and FL1106 for 12.5 kHz channel spacing). Selection of the appropriate filter pair is accomplished by U1101 and U1102, controlled by the BWSELECT line from pin 48 of the synthesizer IC U1201. The filtered output from the ceramic filters is applied to the limiter input pin of the IF IC (pin 14).
The IF IC contains a quadrature detector using a ceramic phase-shift element (Y1102) to provide audio detection. Internal amplification provides an audio output level of 120 mV rms (at 60% deviation) from U1103 pin8 (AUDIOOUT) which is fed to the ASFIC_CMP (U0221) pin 2 (part of the Controller circuitry).
A received signal strength indicator (RSSI) signal is available at U1103 pin 5, having a dynamic range of 70 dB. The RSSI signal is interpreted by the microprocessor (U0101 pin 63) and in addition is available at accessory connector J0501-15.

2.6 “Extender” (Noise Blanker)

The 10.7 MHz output from the first mixer, which is present at the input of first IF amp Q1101, is also routed to the input of the “Extender” (noise blanker) circuitry and amplified by FET Q1610. The high input impedance of the FET stage minimizes loading of the signal in the receiver path. The output of Q1610 is further amplified by U1601, which is a wide-bandwidth, high gain differential amplifier (used in a single-ended configuration) incorporating an AGC gain control input. This gain block provides linear amplification of the instantaneous amplitude of the 10.7 MHz signal at the first mixer output. The output of U1601 is coupled to biased-detector Q1603. The bias is set so that noise impulses of a sufficient amplitude cause Q1603 to conduct. The following stages (Q1604 through Q1606) provide additional gain and pulse shaping which slows the turn-on and turn-off waveform applied to IF blanker switches Q1102 and Q1103. The result is that, for each noise impulse, the IF signal is smoothly ramped off and then on again, preventing the pulse from reaching the narrow IF selectivity, where ringing would cause an objectionable spike at the detector of a much longer duration than the original impulse.
If the repetition rate of noise impulses is so rapid that the noise blanker can no longer blank them individually, as indicated by a large increase in high-frequency content at the output of Q1604, stage Q1607 amplifies this level and turns on level detector Q1609. Its output is highly filtered into a DC voltage level which is proportional to the repetition rate of the noise impulses, and this is applied to the AGC input pin 5 of U1601, reducing its gain and therefore the amount of noise pulses which are detected and processed.

3.0 Low Band Transmitter Power Amplifier (PA) 25-60 W

The radio's 60 W PA is a three-stage amplifier used to amplify the output from the VCO to the radio transmit level. The line-up consists of three stages which utilize LDMOS technology. The first stage is pre-driver (U1401) that is controlled by pin 4 of PCIC (U1503) via Q1504 and Q1505 (CNTLVLTG). It is followed by driver stage Q1401, and final stage utilizing two devices (Q1402 and Q1403) connected in parallel. Q1402 and Q1403 are in direct contact with the heat sink.

To prevent damage to the final stage devices, a safety switch has been installed to prevent the transmitter from being keyed with the cover removed.

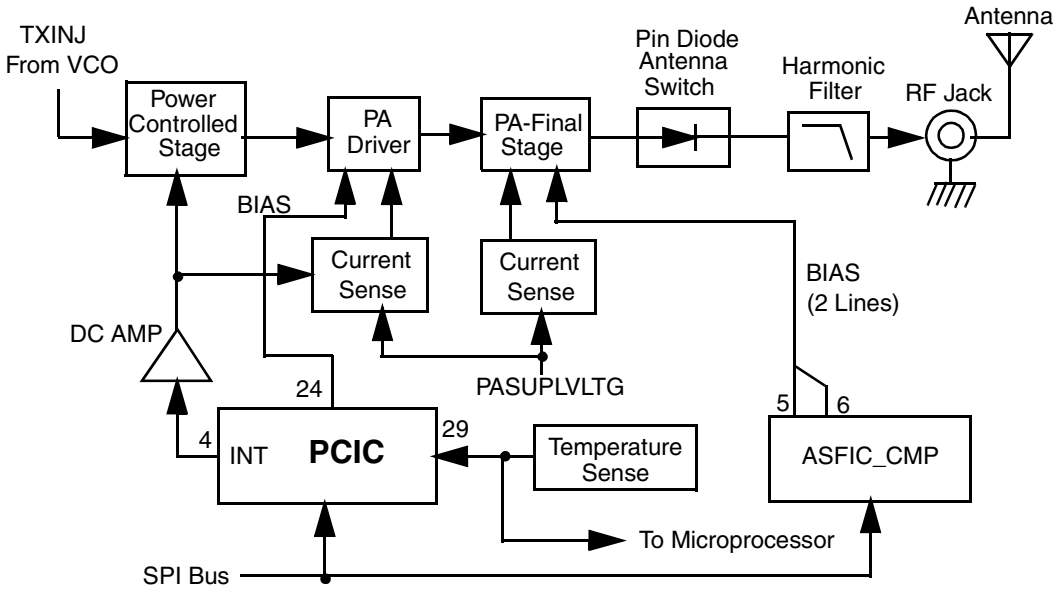


Figure 2-2 LowBand Transmitter Block Diagram

3.1 Power Controlled Stage

The first stage (U1401) is a 20dB gain integrated circuit containing two LDMOS FET amplifier stages. It amplifies the RF signal from the VCO (TXINJ). The output power of stage U1401 is controlled by a DC voltage applied to pin 1 from the power control circuit (U1503 pin 4, with transistors Q1504-5 providing current gain and level-shifting). The control voltage simultaneously varies the bias of two FET stages within U1401. This biasing point determines the overall gain of U1401 and therefore its output drive level to Q1401, which in turn controls the output power of the PA.

3.2 Driver Stage

The next stage is an LDMOS device (Q1401) providing a gain of 13dB. This device requires a positive gate bias and a quiescent current flow for proper operation. The voltage of the line MOSBIAS_1 is set during transmit mode by the PCIC pin 24, and fed to the gate of Q1401 via resistors R1402, R1447, R1449, R1458, R1459 and R1463, The bias voltage is tuned in the factory.

The circuitry associated with U1402-2 and Q1404 limits the variation in the output power of the driver stage resulting from changes in the input impedance of the final stage due to changes at the

antenna of the radio. The variation in the driver's output power is limited by controlling its DC current. The driver's DC current is monitored by measuring the voltage drop across current-sense resistors R1473-6, and this voltage is compared to a reference voltage on pin 6 of U1402-2. If the current through the sense resistors decreases, the circuit increases the bias voltage on the gate of Q1401 via Q1404. If the current increases, then the bias voltage decreases in order to keep the driver's current constant. Since the current must increase with increasing control voltage, an input path is provided to U1402-2 pin 5 from control line VCNTRL to enable this.

3.3 Final Stage

The final stage uses two LDMOS FET devices operating in parallel. Each device has its own adjustable gate bias voltage, MOSBIAS_2 and MOSBIAS_3, obtained from D/A outputs of the ASFIC. These bias voltages are also factory-tuned. If these transistors are replaced, the bias voltage must be tuned using the Tuner Software. Care must be taken not to damage the device by exceeding the maximum allowed bias voltage. The device's drain current is drawn directly from the radio's DC supply voltage input, PASUPVLTG, via current-measurement resistor R1409.

A matching network combines the output of the two devices and provides a 50-ohm source for the antenna switch and harmonic filter.

3.4 Antenna Switch

The antenna switch is operated by the 9T1 voltage source which forward biases diodes D1401 and D1402 during transmit, causing them to appear as a low impedance. D1401 allows the RF output from final stages Q1402 and Q1403 to be applied to the input of the low-pass harmonic filter (L1421-3 and associated components). D1402 appears as a short circuit at the input of the receiver (RXINJ), preventing transmitter RF power from entering the receiver. L1420 and C1456 appear as a broadband _-wave transmission line, making the short circuit presented by D1402 appear as open circuit at the junction of D1401 and the harmonic filter input.

During receive mode, the 9T1 voltage is not present, and D1401 and D1402 do not conduct and appear as open circuits. This allows signals from the antenna jack to pass to the receiver input, and disconnects the transmitter final stages from this path.

3.5 Harmonic Filter

Components L1421-L1423 and C1449-C1455 form a seven-pole elliptic low-pass filter to attenuate harmonic energy of the transmitter to specifications level. R1411 is used to drain electrostatic charge that might otherwise build up on the antenna. The harmonic filter also prevents high level RF signals above the receiver passband from reaching the receiver circuits, improving spurious response rejection.

3.6 Power Control

The transmitter uses the Power Control IC (PCIC, U1503) to control the power output of the radio. A differential DC amplifier U1502-1 compares the voltage drop across current-measuring resistor R1409, which is proportional to the transmitter final stage DC current, with the voltage drop across resistor R1508 and R1535, which is proportional to the current through transistor Q1503. This transistor is controlled by the output of the differential amplifier, which varies the transistor Q1503. This transistor is controlled by the output of the differential amplifier, which varies the transistor

current until equilibrium of the two compared voltages is reached. The current through Q1503 develops a voltage across R1513 which is exactly proportional to the DC current of the final stages. This voltage is applied to the RF IN port of the PCIC (pin 1).

The PCIC has internal digital to analog converters (DACs) which provide a reference voltage of the control loop. The reference voltage level is programmable through the SPI line of the PCIC. This reference voltage is proportional to the desired power setting of the transmitter, and is factory programmed at several points across the frequency range of the transmitter to offset frequency response variations of the transmitter's power detector circuitry.

The PCIC provides a DC output voltage at pin 4 (INT) which is amplified and shifted in DC level by stages Q1504 and Q1505. The 0 to 4 volt DC range at pin 4 of U1503 is translated to a 0 to 8 volt DC range at the output of Q1505, and applied as VCNTRL to the power-adjust input pin of the first transmitter stage U1401. This adjusts the transmitter power output to the intended value. Variations in antenna impedance cause variations in the DC current of the final stages, and the PCIC adjusts the control voltage above or below its nominal value to reduce power if current drain increases, or raise power if current drain decreases.

Capacitors C1503-4 and C1525, in conjunction with resistors and integrators within the PCIC, control the transmitter power-rise (key-up) and power-decay (de-key) characteristic to minimize splatter into adjacent channels.

U1501 is a temperature-sensing device which monitors the circuit board temperature in the vicinity of the transmitter circuits and provides a dc voltage to the PCIC (TEMP, pin 29) proportional to temperature. If the DC voltage produced exceeds the set threshold in the PCIC, the transmitter output power will be reduced so as to reduce the transmitter temperature.

3.7 TX Safety Switch

The TX Safety Switch consists of S1501, Q1506, and diode pairs D1502 and D1503 providing protection to the Þnal stage divices Q1402 and Q1403. These Þnal stage devices can be degraded or destroyed if the radio is keyed without the cover in place due to the lack of a good thermal path to the chassis.

Switch S1501 is closed when the radio´s cover is screwed in place by means of the carbonized reqion on the cover´s pressure pad making contact with the Þnger plating on the radio´s PCB. With the cover in place, transistor Q1506 is off, back-biasing diodes D1502 and D1503, enabling proper transmitter operation. When the cover is not in place, S1501 opens, causing Q1506 to rurn on, pulling the cathodes of D1502 and D1503 to ground, resulting in the shorting of the transmitter´s bias lines and control voltage.

4.0 Low Band Frequency Synthesis

The frequency synthesizer subsystem consists of the reference oscillator crystal (Y1201), the Low Voltage Fractional-N synthesizer (LVFRAC-N, U1201), and the receive and transmit VCOs and buffers (Q1303 through Q1308 and associated components).

4.1 Fractional-N Synthesizer

The LVFRAC-N synthesizer IC (U1201) consists of a reference oscillator, pre-scaler, a programmable loop divider, control divider logic, a phase detector, a charge pump, an A/D converter

for low frequency digital modulation, a balance attenuator to balance the high frequency analog modulation and low frequency digital modulation, a 13V positive voltage multiplier, a serial interface for control, and finally a super filter for the regulated 9.3 volt supply.

Regulated 9.3 volts DC applied to the super filter input (U1201 pin 30) delivers a very low noise output voltage of 8.3 volts DC (VSF) at pin 28. External device Q1201 allows greater current sourcing capability. The VSF source supplies the receive and transmit VCOs and first buffer stages. The synthesizer IC supply voltage is provided by a dedicated 5V regulator (U1250) to minimize power supply noise.

In order to generate a high voltage to supply the phase detector (charge pump) output stage at pin VCP (U1201 pin 47), a capacitive voltage multiplier circuit (CR1202 and C1209) generates a voltage of 13 volts DC. This multiplier is driven by two 1.05 MHz clock signals from U1201 pins 15 and 14 (VMULT1 and VMULT2) which are 180° out of phase.

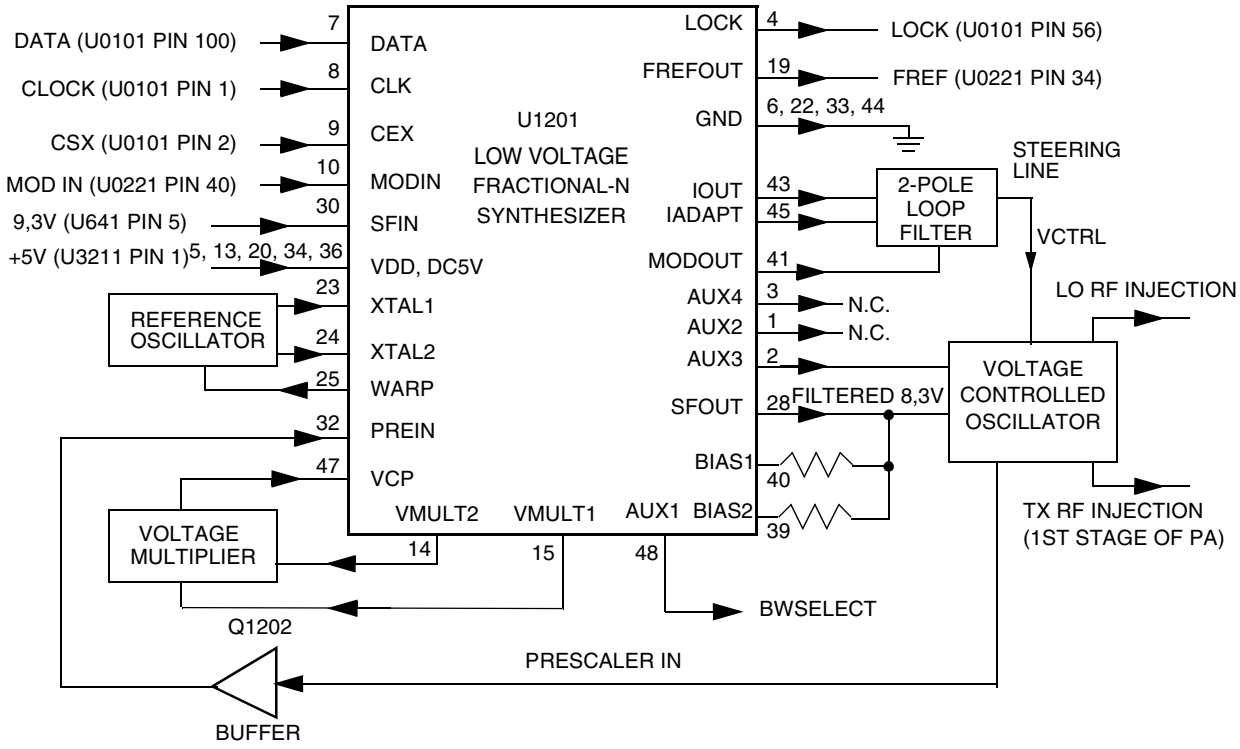


Figure 2-3 LowBand Synthesizer Block Diagram

Output LOCK (U1201-4) provides information about the lock status of the synthesizer loop. A high level at this output indicates a stable loop. A buffered output of the 16.8 MHz reference frequency is provided at pin 19.
The operating frequency of the synthesizer is loaded serially from the microprocessor via the data line (DATA, U1201-7), clock line (CLK, U1201-8) and chip select line (CSX, U1201-9).
The reference oscillator circuit within U1201 uses an external 16.8 MHz crystal (Y1201). Varactor CR1201 allows software-controlled frequency adjustment (warp) and temperature compensation of the oscillator frequency. Warp adjustment is performed using serial data from the microprocessor. This controls the setting of an A/D converter, with its output (WARP, pin 25) applied to CR1201.

4.2 Voltage Controlled Oscillator (VCO)

Separate VCO and buffer circuits are used for receiver injection and transmitter carrier frequency generation. Since the receiver uses high-side injection, the receiver VCO frequency range is 10.7 MHz above the transmit VCO range. The VCO/buffers are bandsplit into three ranges depending on radio model, covering radio operating frequencies of 29.7 to 36.0 MHz, 36.0 to 42.0 MHz, or 42.0 to 50.0 MHz. The corresponding three frequency ranges for the receive VCO are 40.4 to 46.7 MHz, 46.7 to 52.7 MHz, and 52.7 to 60.7 MHz.

The VCOs, together with Fractional-N synthesizer U1201, generate the required frequencies for transmit and receive mode. The TRB line (U1201 pin 2) determines which VCO/buffer circuit is to be enabled. A high level on TRB will turn on the transistors in U1378 to turn on via R1376, applying the 8.3 volt VSF source to the receiver VCO and first buffer. The second buffer in each string operates from the 9V3 source and become active when RF is applied to their inputs.
The RF signal at the bases of the second buffers are combined and fed back to the Fractional-N synthesizer via PRE_IN where it is compared to the reference frequency as described below in “Synthesizer Operation”. The Fractional-N IC provides a DC steering voltage VCTRL to adjust and maintain the VCO at the correct frequency.
With a steering voltage from 2.5V to 11V at the appropriate varactor diode (CR1302 for the RX VCO, or CR1310 for the TX VCO), the full VCO tuning range is obtained. Each VCO uses and AGC circuit to maintain a constant VCO output level across the frequency band. A diode (CR1306 in the receive VCO, or CR1314 in the transmit VCO) is configured as a voltage doubler which rectifies the RF level sampled at the VCO drain and applies a proportional negative DC voltage to the VCO gate. Increased RF level reduces the VCO gain to compensate.

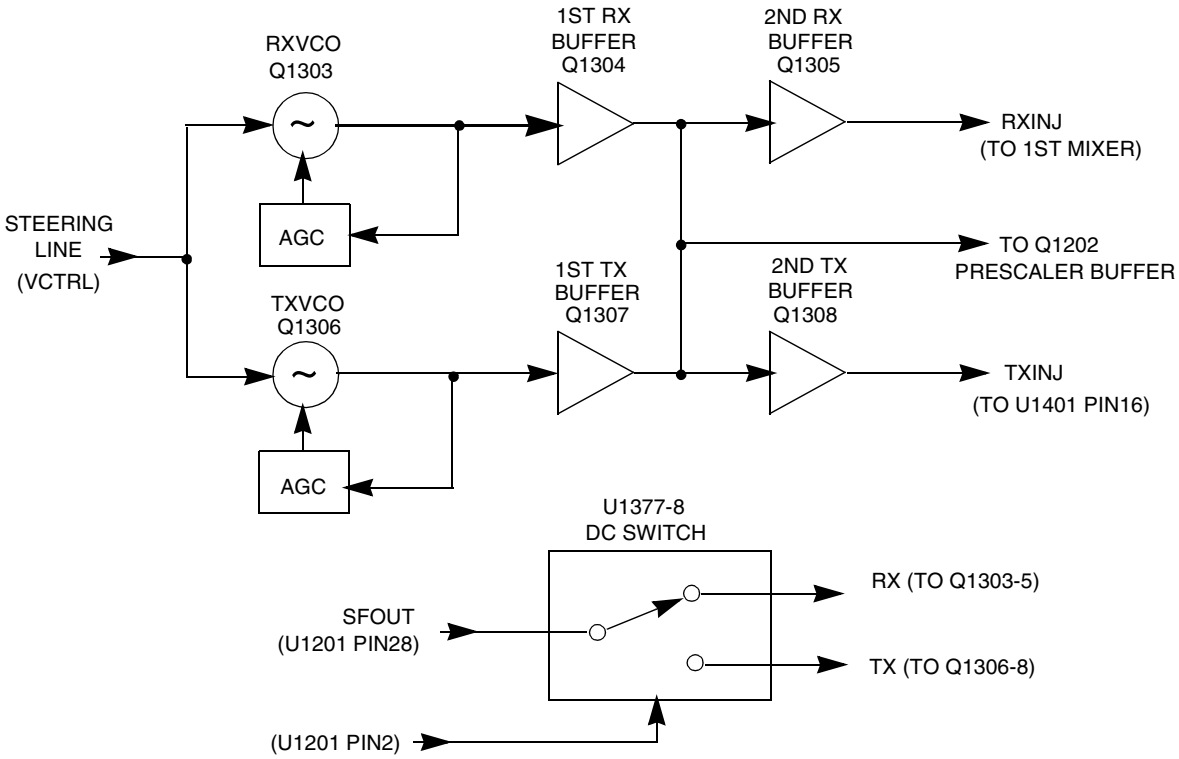


Figure 2-4 LowBand VCO/Buffer Block Diagram

The VCO output is taken from the source and applied to the first buffer transistor (Q1304 receive, Q1307 transmit). The first buffer output is further amplified by the second buffer transistor (Q1305 Rx, Q1308 Tx) before being applied to the receiver first mixer or transmitter first stage input.
In TX mode the modulation signal coming from the LVFRAC-N synthesizer IC (MODOUT, U1201 pin 41) is superimposed on the DC steering line voltage by capacitive divider C1215, C1208 and C1212, causing modulation of the TX VCO using the same varactor as used for frequency control.

4.3 Synthesizer Operation

The complete synthesizer subsystem comprises mainly of low voltage LVFRAC-N synthesizer IC, Reference Oscillator (crystal oscillator with temperature compensation), charge pump circuitry, loop filter circuitry, and voltage-controlled oscillators and buffers. A sample of the VCO operating signal PRE_IN is amplified by feedback buffer Q1202, low-pass filtered by L1205, C1222 and C1224, and fed to U1201 pin 32 (PREIN).

The pre-scaler in the synthesizer (U1201) is basically a dual modulus pre-scaler with selectable divider ratios. This divider ratio of the pre-scaler is controlled by the loop divider, which in turn receives its inputs via the serial interface to the microprocessor. The output of the pre-scaler is applied to the loop divider. The output of the loop divider is connected to the phase detector, which compares the loop divider´s output signal with the reference signal. The reference signal is generated by dividing down the signal of the reference oscillator, whose frequency is controlled by Y1201.

The output signal of the phase detector is a pulsed DC signal which is routed to the charge pump. The charge pump outputs a current at pin 43 of U1201 (I OUT). The loop filter (which consists of R1205-6, R1208, C1212-14) transforms this current into a voltage that is applied to the varactor diodes (CR1310 for transmit, CR1302 for receive) and alters the output frequency of the appropriate VCO. The current can be set to a value fixed in the LVFRAC-N IC or to a value determined by the currents flowing into BIAS 1 (U1201-40) or BIAS 2 (U1201-39). The currents are set by the value of R1211 or R1207 respectively. The selection of the three different bias sources is done by software programming.

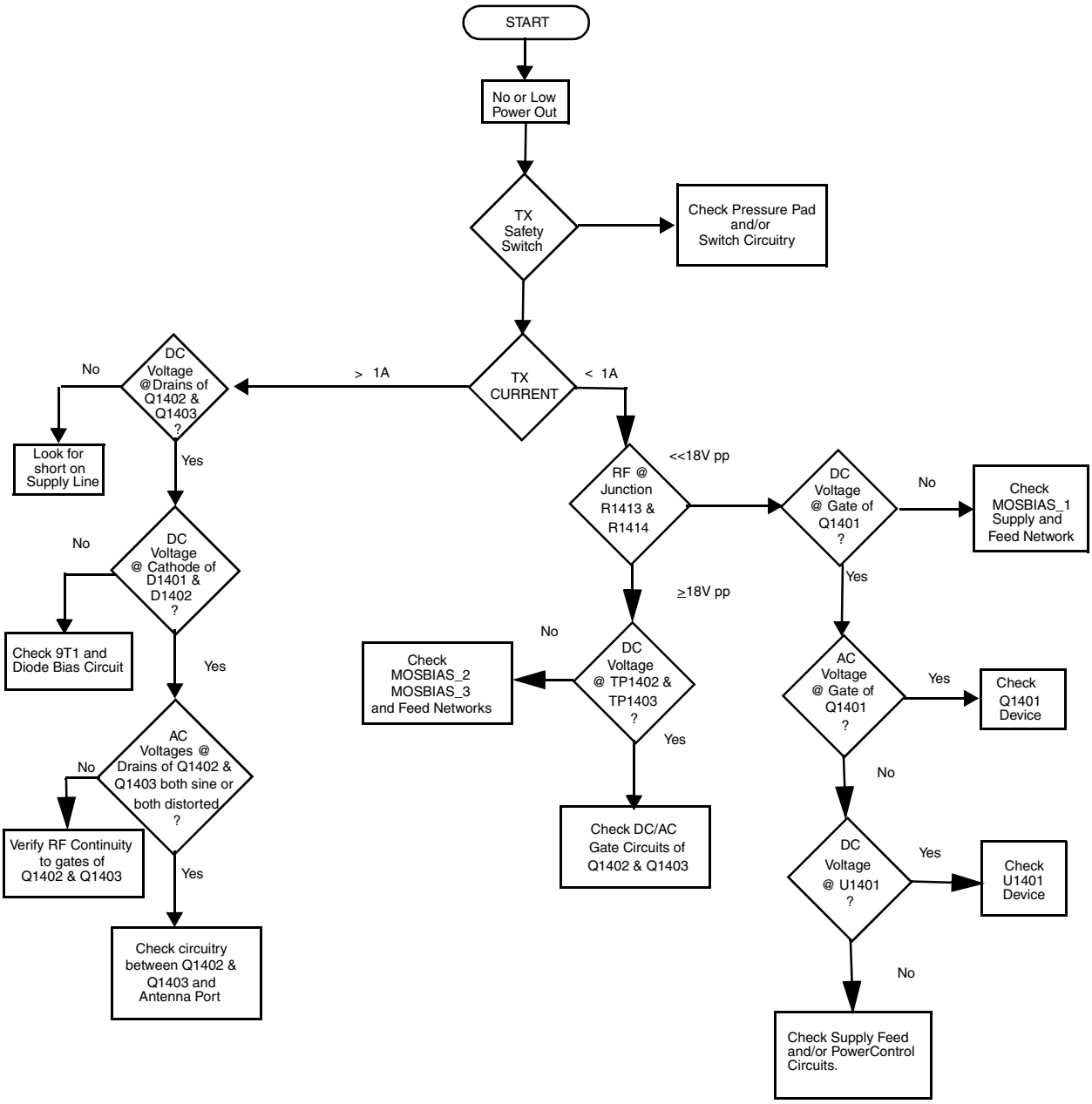
To reduce synthesizer lock time when new frequency data has been loaded into the synthesizer the magnitude of the loop current is increased by enabling the IADAPT (U1201-45) for a certain software programmable time (Adapt Mode). The adapt mode timer is started by a low to high transient of the CSX line. When the synthesizer is within the lock range the current is determined only by the resistors connected to BIAS 1, BIAS 2, or the internal current source. A settled synthesizer loop is indicated by a high level of signal LOCK (U1201-4).

In order to modulate the PLL the two spot modulation method is utilized. Via pin 10 (MODIN) on U1201, the audio signal is applied to both the A/D converter (low frequency path) and the balanced attenuator (high frequency path). The A/D converter converts the low frequency analog modulating signal into a digital code that is applied to the loop divider, thereby causing the carrier to deviate. The balance attenuator is used to adjust the VCO's deviation sensitivity to high frequency modulating signals. The output of the balance attenuator is present at the MODOUT port (U1201-41) and superimposed on the VCO steering line voltage by a divider consisting of C1215, C1208 and C1212.

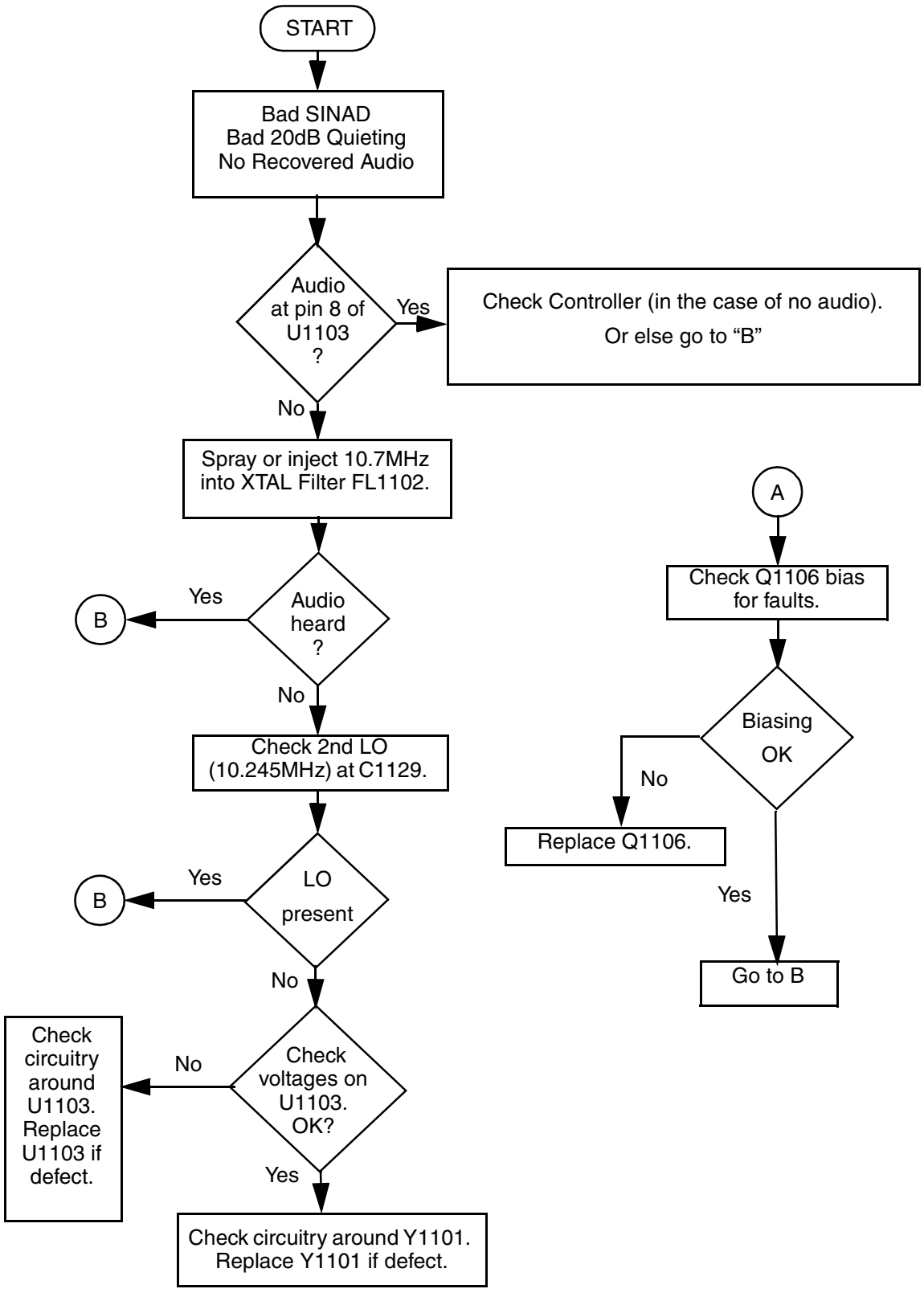
Chapter 3

LOW BAND TROUBLESHOOTING CHARTS

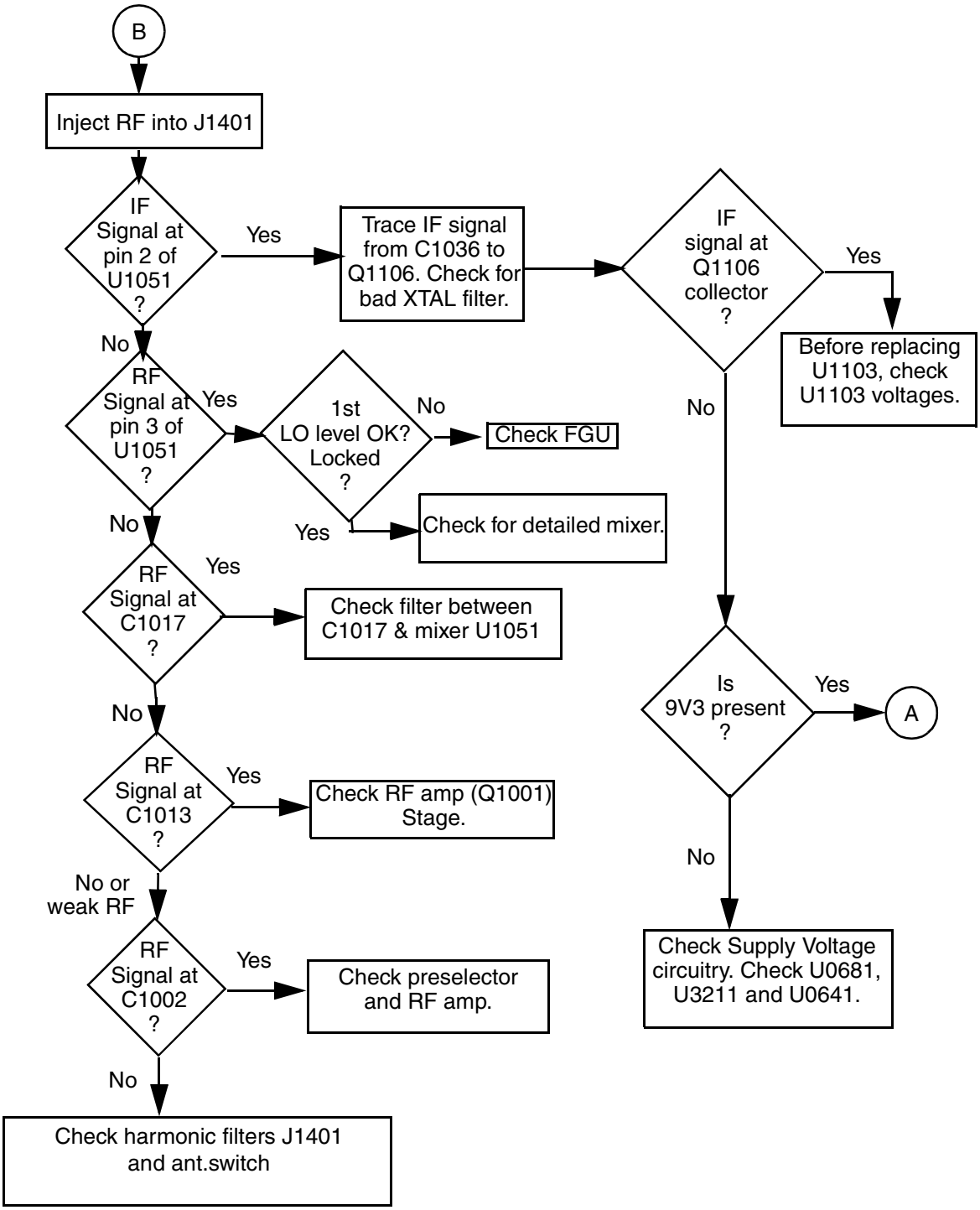
1.0 Troubleshooting Flow Chart for Transmitter



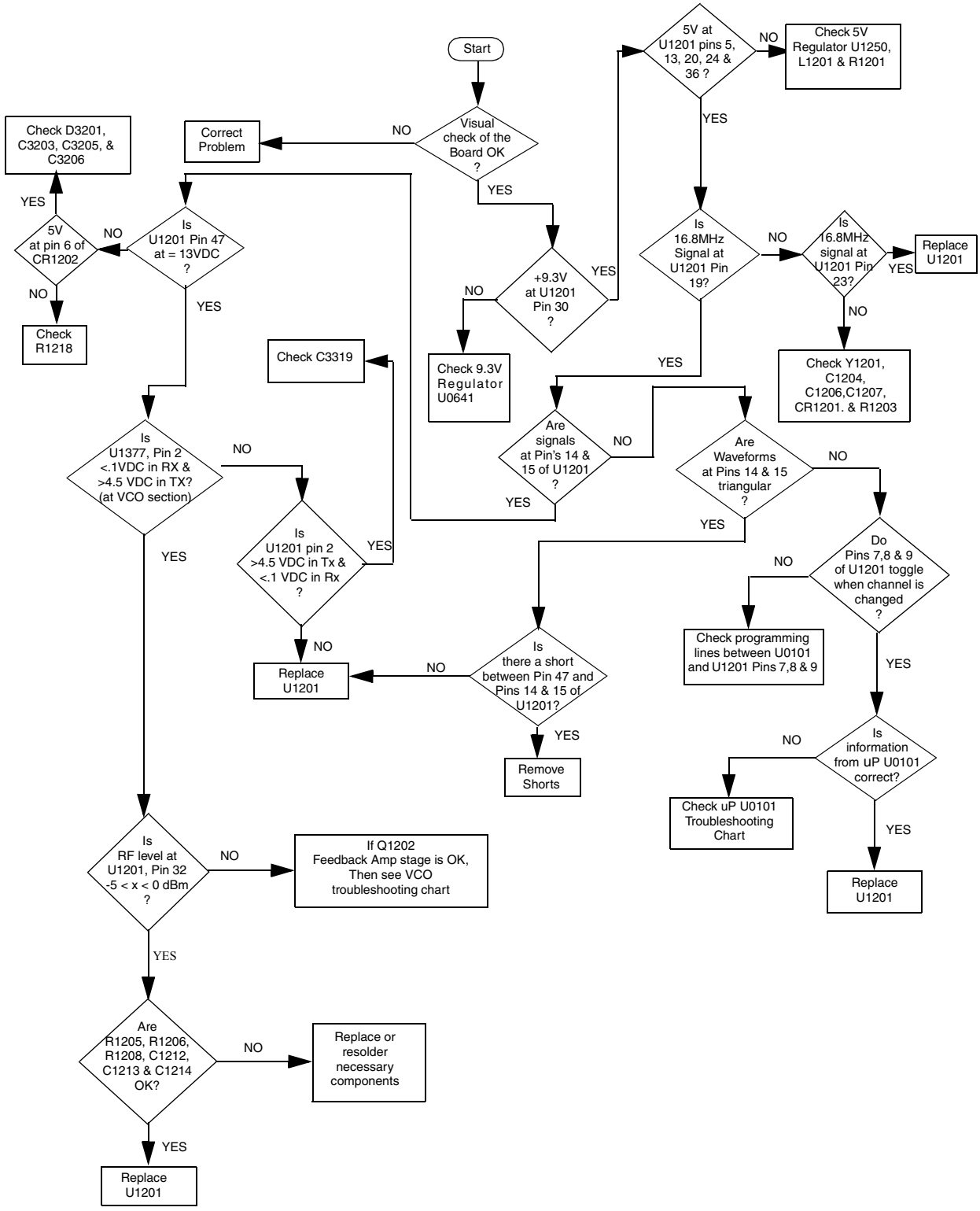
2.0 Troubleshooting Flow Chart for Receiver (Sheet 1 of 2)



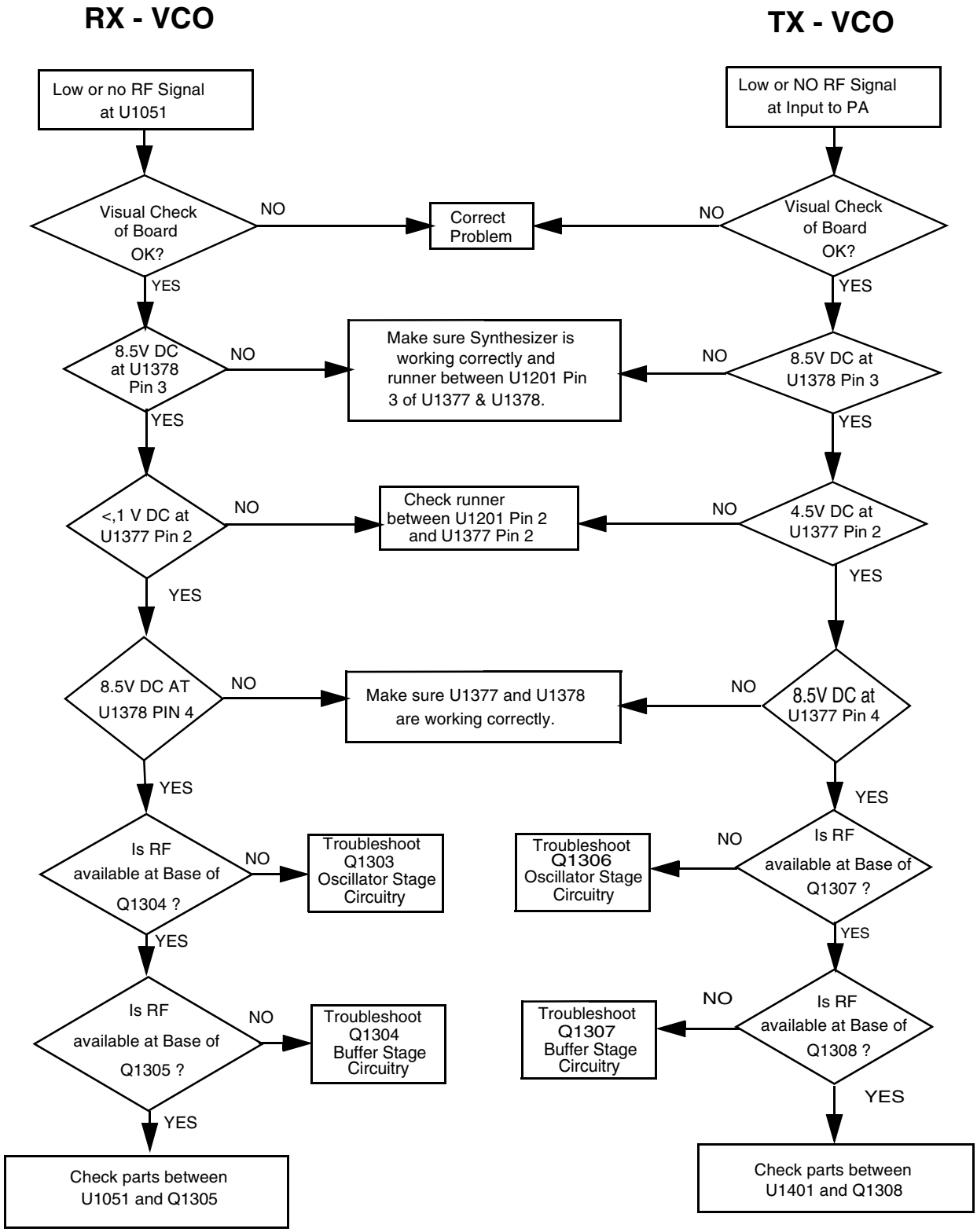
Troubleshooting Flow Chart for Receiver (Sheet 2 of 2)



3.0 Troubleshooting Flow Chart for Synthesizer



4.0 Troubleshooting Flow Chart for VCO



Chapter 4

LOW BAND PCB/SCHEMATICS/PARTS LISTS

1.0 Allocation of Schematics and Circuit Boards

1.1 Controller Circuits

The Low Band circuits are contained on the printed circuit board (PCB) which also contains the Controller circuits. This Chapter shows the schematics for the Low Band circuits only, refer to the Controller section for details of the related Controller circuits . The PCB component layouts and the Parts Lists in this Chapter show both the Controller and Low Band circuit components.
The Low Band schematics and the related PCB and parts list are shown in the tables below.

Table 4-1 LB1 25-60W Diagrams and Parts Lists

Table 4-2 LB2 25-60W Diagrams and Parts Lists

Table 4-3 LB3 25-60W Diagrams and Parts Lists

Table 4-4 LB1 25-60W Diagrams and Parts Lists

Table 4-5 LB2 25-60W Diagrams and Parts Lists

PCB :	
8486207B07 Main Board Top Side	Page 4-51
8486207B07 Main Board Bottom Side	Page 4-52
SCHEMATICS	
Power Amplifier 25-60W (Sheet 1 of 2)	Page 4-20
Power Amplifier 25-60W (Sheet 2 of 2)	Page 4-21
Voltage Controlled Oscillator	Page 4-22
Receiver Front End	Page 4-23
IF (Sheet 1 of 2)	Page 4-46
IF (Sheet 2 of 2)	Page 4-47
Noise Blanker	Page 4-26
FRACN	Page 4-27
Parts List	
8486207B07	Page 4-53
Controller version is **T11**	

Table 4-6 LB3 25-60W Diagrams and Parts Lists

PCB :	
8485908z04 Main Board Top Side	Page 4-56
8485908z04 Main Board Bottom Side	Page 4-57
SCHEMATICS	
Power Amplifier 25-60W (Sheet 1 of 2)	Page 4-33
Power Amplifier 25-60W (Sheet 2 of 2)	Page 4-34
Voltage Controlled Oscillator	Page 4-35
Receiver Front End	Page 4-36
IF (Sheet 1 of 2)	Page 4-46
IF (Sheet 2 of 2)	Page 4-47
Noise Blanker	Page 4-39
FRACN	Page 4-40
Parts List	
8485908z04	Page 4-58
Controller version is **T11**	